AMENDMENTS

In The Claim:

Claim 1 (original) A method of manufacturing a metal-oxide-semiconductor (MOS) transistor, comprising the steps of:

providing a substrate having a gate structure thereon;

forming a first spacer on the sidewall of the gate structure;

performing a pre-amorphization implantation to amorphize a portion of the substrate;

forming a doped source/drain extension region in the substrate on each side of the first spacer;

forming a second spacer on the sidewall of the first spacer;

forming a doped source/drain region in the substrate on each side of the second spacer;

performing a pre-annealing process; and

performing a solid phase epitaxial process to re-crystallize the amorphized portion of the substrate and activate the doped source/drain extension region and the doped source/drain region to form a source/drain terminal, wherein the annealing temperature in the pre-annealing operation is lower than the operating temperature in the solid phase epitaxial process.

Claim 2 (original) The method of claim 1, wherein the pre-annealing process comprises placing the substrate inside a furnace and heating up the furnace.

Claim 3 (original) The method of claim 1, wherein the pre-annealing process comprises heating to an annealing temperature between about 400°C to 500°C.

Claim 4 (original) The method of claim 3, wherein the pre-annealing process comprises maintaining the substrate at the annealing temperature for a period of about 30 minutes.

Claim 5 (currently amended) A method of manufacturing a metal-oxide-semiconductor (MOS) transistor, comprising the steps of:

providing a substrate having a gate structure thereon;

forming a first spacer on the sidewall of the gate structure;

performing a pre-amorphization implantation to amorphize a portion of the substrate;

forming a doped source/drain extension region in the substrate on each side of the first spacer;

forming a second spacer on the sidewall of the first spacer;

forming a doped source/drain region in the substrate on each side of the second spacer;

performing a solid phase epitaxial process to re-crystallize the amorphized portion of the substrate and activate the doped source/drain extension region and the doped source/drain region to form a source/drain terminal~~, wherein the annealing temperature in the pre-annealing operation is lower than the operating temperature in the solid phase epitaxial process~~; and

performing a post-annealing process, wherein the annealing temperature in the post-annealing operation is higher than the operating temperature in the solid phase epitaxial process.

Claim 6 (original) The method of claim 5, wherein the post-annealing operation comprises performing a rapid thermal annealing process.

Claim 7 (original) The method of claim 5, wherein the post-annealing process comprises heating the substrate to an annealing temperature of about 850°C.

Claim 8 (original) The method of claim 7, wherein the post-annealing process comprises maintaining the substrate at the annealing temperature for a period of about 20

seconds.

Claim 9 (original) The method of claim 5, wherein the post-annealing process comprises heating the substrate to an annealing temperature between about 900°C to 1000°C.

Claim 10 (original) The method of claim 9, wherein the post-annealing process comprises maintaining the substrate at the annealing temperature for a spike period.

Claim 11 (original) A method of manufacturing a metal-oxide-semiconductor (MOS) transistor, comprising the steps of:

providing a substrate having a gate structure thereon;

forming a first spacer on the sidewall of the gate structure;

performing a pre-amorphization implantation to amorphize a portion of the substrate;

forming a doped source/drain extension region in the substrate on each side of the first spacer;

forming a second spacer on the sidewall of the first spacer;

forming a doped source/drain region in the substrate on each side of the second spacer;

performing a pre-annealing process;

performing a solid phase epitaxial process to re-crystallize the amorphized portion of the substrate and activate the doped source/drain extension region and the doped source/drain region to form a source/drain terminal, wherein the annealing temperature in the pre-annealing operation is lower than the operating temperature in the solid phase epitaxial process; and

performing a post-annealing process, wherein the annealing temperature in the post-annealing operation is higher than the operating temperature in the solid phase epitaxial process.

Claim 12 (original) The method of claim 11, wherein the pre-annealing process comprises placing the substrate inside a furnace and heating up the furnace.

Claim 13 (original) The method of claim 11, wherein the pre-annealing process comprises heating to an annealing temperature between about 400°C to 500°C.

Claim 14 (original) The method of claim 13, wherein the pre-annealing process comprises maintaining the substrate at the annealing temperature for a period of about 30 minutes.

Claim 15 (original) The method of claim 11, wherein the post-annealing operation comprises performing a rapid thermal annealing process.

Claim 16 (original) The method of claim 11, wherein the post-annealing process comprises heating the substrate to an annealing temperature of about 850°C.

Claim 17 (original) The method of claim 16, wherein the post-annealing process comprises maintaining the substrate at the annealing temperature for a period of about 20 seconds.

Claim 18 (original) The method of claim 11, wherein the post-annealing process comprises heating the substrate to an annealing temperature between about 900°C to 1000°C.

Claim 19 (original) The method of claim 18, wherein the post-annealing process comprises maintaining the substrate at the annealing temperature for a spike period.